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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,486	10/15/2003	Robin Cheung	AMAT/3421.C2/CMP/ECP/RKK	8014

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EXAMINER	
WILKINS III, HARRY D	

ART UNIT	PAPER NUMBER
1742	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/686,486	CHEUNG ET AL.	
	Examiner	Art Unit	
	Harry D. Wilkins, III	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status

1. The double patenting type rejections have been withdrawn in view of Applicant's filing of terminal disclaimers.

2. The rejection of claim under 35 USC 112, 2nd paragraph has been withdrawn in view of Applicant's correction of claim 1.

Terminal Disclaimer

3. The terminal disclaimers filed on 17 April 2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent 6,635,157 or any Patent granted on Application No. 10/972,884 or 11/114,936 have been reviewed and are accepted. The terminal disclaimers have been recorded.

Priority

4. Applicant's remarks filed 17 April 2006 assert an effective filing date of 5 March 1999. However, the specification does not support such a claim. The only priority claim contained in the present Application is to 09/607,347, filed 5 July 2000. Applicant appears to be attempting to rely on the filing date of 09/263,126, however, no priority claim to that Application has been made in the present Application. Applicant is also reminded of the changes to 37 CFR 1.78 requiring a petition to add unintentionally delayed benefit claims.

5. Therefore, the present Application is granted an effective filing date of 5 July 2000 since that is the earliest date to which priority has been claimed.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 19 recites the limitation "the one or more loading station robots" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dordi et al (US 6,258,220, US 2004/0084301, 2002/0029961, 6,635,157).

The applied reference has common assignee and inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this

application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

[Each of the further references are related as continuations or divisionals of application no. 09/289,074, which published as US patent 6,258,220.]

11. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dordi et al (US 6,267,853).

The applied reference has common assignee and inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

12. Claims 10, 11, 17 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hanson et al (US 6,091,498).

Hanson et al anticipate the invention as claimed. Hanson et al teach (see figures 1, 2, 10 and 11) a semiconductor wafer electrochemical deposition system including a mainframe (10) having a wafer transfer robot (64) therein, a loading station (12) disposed in connection with the mainframe with a loading station robot (62), multiple electrochemical deposition cells (810, figure 11) and multiple rinse and dry stations (805, figure 11 and col. 9) for post-deposition treatment of the semiconductor wafer.

Regarding claim 11, the loading station included multiple wafer cassette receiving areas and a wafer orientor (850, figure 11).

Regarding claim 17, Hanson et al teach (see figure 11) an electrochemical deposition system including a mainframe having a mainframe wafer transfer robot disposed therein, a loading station disposed in connection with the mainframe with multiple cassette receiving areas, multiple electrochemical deposition stations and multiple post deposition treatment chambers in connection with the loading station.

Regarding claim 18, Hanson et al teach (see figure 11) that the post deposition treatment chamber were rinse-dry modules.

13. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Curtis et al (US 6,264,752).

Curtis et al anticipate the invention as claimed. Curtis et al teach (see figure 12 and col. 10, lines 10-36) an electrochemical deposition system including a mainframe having a mainframe wafer transfer robot therein, a loading station having cassette receiving areas (S.M.I.F pods) two or more electrochemical deposition processing stations and two or more post treatment clean/dry stations (i.e.-spin-rinse-dry stations).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis et al (US 6,264,752) in view of Uzoh et al (US 6,123,825).

Curtis et al teach (see figure 12) a wafer processing apparatus including a mainframe with a wafer transfer robot (625), a loading station (607) and multiple processing stations (605) which included electrodeposition cells (see col. 10, lines 10-36) which would necessarily require an electrolyte fluid supply connected to the cell.

Thus, Curtis et al fail to teach including a thermal anneal chamber disposed adjacent the loading station.

Uzoh et al teach (see paragraph spanning cols. 7 and 8) annealing of copper electroplated wafers for the purpose of improving grain structure of the electroplated copper.

Therefore, it would have been obvious to one of ordinary skill in the art to have used a thermal anneal chamber for performing the annealing as taught by Uzoh et al in the apparatus of Curtis et al. Though Uzoh et al do not teach positioning the annealing station adjacent the loading station, it would have been obvious to have placed the station at any convenient location with respect to the apparatus without affecting the operation of the apparatus.

Regarding claim 4, it would have been obvious to one of ordinary skill in the art to have added a system controller to the electrodeposition cell of Curtis et al in order to provide precise control over the operating parameters.

16. Claims 2, 3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis et al (US 6,264,752) in view of Uzoh et al (US 6,123,825) as applied to claims 1 and 4 above, and further in view of Moore et al (US 6,151,447).

The teachings of Curtis et al and Uzoh et al are described above.

Uzoh et al contains no details with respect to the thermal anneal chamber.

Moore et al teach (see abstract and figures) a thermal anneal chamber useful for processing wafers.

Therefore, it would have been obvious to one of ordinary skill in the art to have used the thermal anneal chamber of Moore et al to perform the annealing treatment taught by Uzoh et al because the annealing chamber of Moore et al provided lowered process times by providing rapid heating.

Regarding claim 2, the annealing chamber of Moore et al included a heat plate (327).

Regarding claim 3, the annealing chamber of Moore et al would have been capable of operating at atmospheric pressure.

Regarding claim 5, the annealing chamber of Moore et al included a gas inlet.

Regarding claim 6, it would have been obvious to one of ordinary skill in the art to have adapted the system controller to have controlled the oxygen content of the gas in the annealing chamber to be less than 100 ppm in order to prevent the electroplated copper layer from becoming oxidized.

Regarding claims 7 and 8, Uzoh et al suggests performing the annealing treatment in a hydrogen-nitrogen atmosphere. Therefore, it would have been obvious to

one of ordinary skill in the art to have adapted the annealing chamber of Moore et al to input nitrogen and hydrogen gases. It would have been within the expected skill of a routineer in the art to have optimized the ratio of hydrogen to oxygen of the annealing atmosphere.

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis et al (US 6,264,752) in view of Uzoh et al (US 6,123,825) as applied to claims 1 and 4 above, and further in view of Togawa et al (US 5,830,045).

The teachings of Curtis et al are described above. The device of Curtis included multiple wafer transfer robots capable of transferring the wafers to different locations.

Curtis et al are silent with respect to wafer cassettes being utilized and a wafer orientor being used.

However, Togawa et al teach (see figure 1 and abstract) using wafer cassettes for a wafer processing apparatus and including a loading station robot for transferring wafers from the loading station to a first processing station. Togawa et al also teach a wafer orientor (5) for ensuring proper orientation of the wafers.

Therefore, it would have been obvious to one of ordinary skill in the art to have adapted the apparatus of Curtis et al to receive wafer cassettes as taught by Togawa et al in order to decrease labor required to run the reactor by reducing the number of times the operator would have to load wafers into the apparatus. It would have been obvious to one of ordinary skill in the art to have added a loading station wafer transfer robot as suggested by Togawa et al to improve productivity of the system. It would have been obvious to one of ordinary skill in the art to have added a wafer orientor as taught by

Togawa et al to the apparatus of Curtis et al to have ensured proper orientation of the wafers.

18. Claims 10, 11, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Uzoh et al (US 6,123,825).

Yoshioka et al teach (see figure 1) a system for treatment of semiconductor wafers including a mainframe (12) having a transfer robot (14) therein, a loading station (30) disposed in connection with the mainframe (12), wherein the loading station included a transfer robot (38) and multiple processing stations (20-24) in connection with the mainframe.

However, Yoshioka et al do not teach that the processing stations included one or more electrochemical deposition cells and one or more post deposition treatment chambers.

Bleck et al teach (see abstract and figure 1) processing stations for semiconductor wafers wherein an electrochemical deposition treatment was carried out.

Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated the electrochemical deposition chambers of Bleck et al into the mainframe wafer processing system of Yoshioka et al in order to allow more complete processing of the wafers within the single system.

Uzoh et al teach (see cols. 7-8) that after formation of an electroplated copper layer on semiconductor wafers, it was customary to perform annealing of the copper layer to ensure small grain size of the copper within the layer.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a conventional post deposition treatment annealing chamber to the system of Yoshioka et al and Bleck et al in order to perform the conventional annealing step to ensure proper grain size of the electroplated copper layer.

Regarding claim 11, the system of Yoshioka et al included two cassette receiving areas and a wafer orientor (38).

Regarding claim 15, Uzoh et al suggest using thermal annealing chambers as the post deposition treatment chambers.

Regarding claim 17, the system of Yoshioka et al included multiple identical processing stations to allow an increased throughput by parallel processing of wafers at the different stations.

19. Claims 10-13 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Shinbara (US 6,155,275).

Yoshioka et al teach (see figure 1) a system for treatment of semiconductor wafers including a mainframe (12) having a transfer robot (14) therein, a loading station (30) disposed in connection with the mainframe (12), wherein the loading station included a transfer robot (38) and multiple processing stations (20-24) in connection with the mainframe.

However, Yoshioka et al do not teach that the processing stations included one or more electrochemical deposition cells and one or more post deposition treatment chambers.

Bleck et al teach (see abstract and figure 1) processing stations for semiconductor wafers wherein an electrochemical deposition treatment was carried out.

Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated the electrochemical deposition chambers of Bleck et al into the mainframe wafer processing system of Yoshioka et al in order to allow more complete processing of the wafers within the single system.

Shinbara teaches (see figure 1 and related description) a wafer processing apparatus including a spin-rinse-dry station (U3) for cleaning the wafers after processing.

Therefore, it would have been obvious to one of ordinary skill in the art to have included a spin-rinse-dry station as taught by Shinbara in the apparatus of Yoshioka et al and Bleck et al for the purpose of cleaning the wafers after the electrodeposition process.

Regarding claim 11, the system of Yoshioka et al included two cassette receiving areas and a wafer orientor (38).

Regarding claims 12 and 13, Shinbara teaches using spin-rinse-dry stations. However, Shinbara does not teach that the loading station robot transferred wafers from the cassettes to the spin-rinse-dry modules. However, it would have been obvious to one of ordinary skill in the art to have placed the stations at any convenient location with respect to the loading station robot without otherwise affecting the operation of the apparatus. See MPEP 2144.04.VI.C. A motivation to perform this rearrangement would be to allow easy access for preliminary rinsing/cleaning and for final

rinsing/cleaning of processed wafers, such that the first and last station the wafers are treated at are the spin-rinse-dry stations.

Regarding claim 17, the system of Yoshioka et al included multiple identical processing stations to allow an increased throughput by parallel processing of wafers at the different stations.

Regarding claim 18, Shinbara teaches using spin-rinse-dry stations.

Regarding claim 19, Shinbara does not teach that the loading station robot transferred wafers from the cassettes to the spin-rinse-dry modules. However, it would have been obvious to one of ordinary skill in the art to have placed the stations at any convenient location with respect to the loading station robot without otherwise affecting the operation of the apparatus. See MPEP 2144.04.VI.C. A motivation to perform this rearrangement would be to allow easy access for preliminary rinsing/cleaning and for final rinsing/cleaning of processed wafers, such that the first and last station the wafers are treated at are the spin-rinse-dry stations.

20. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Uzoh et al (US 6,123,825) OR Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Shinbara (US 6,155,275) as applied to claim 10 above, and further in view of Gonzalez-Martin et al (US 6,213,853).

The teachings of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara are described above. However, none of these references teach that one of the mainframe

transfer robots facilitates transfer of a wafer from a face-up position to a face-down position.

Gonzalez-Martin et al teach (see col. 7, lines 45-56 and figure 1) a transfer robot for use in semiconductor wafer processing that enables the wafer to be flipped from device side-up to device side-down.

Since the various processes performed by the apparatus of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara require processing in both face-up and face-down orientations, it would have been obvious to one of ordinary skill in the art to have added a flipper as taught by Gonzalez-Martin et al to the system.

21. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Uzoh et al (US 6,123,825) OR Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Shinbara (US 6,155,275) as applied to claim 10 above, and further in view of Ting et al (US 5,997,712).

The teachings of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara are described above. However, none of these references teach that there was an electrolyte replenishing system disposed about the mainframe in fluid communication with each of the electrochemical deposition cells.

Ting et al teach (see abstract and figure 1) a copper electrolyte replenishing system for providing electrolyte to electrochemical deposition cells by replenishing the copper depleted from the electrolyte during electroplating.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a copper electrolyte replenishing system as taught by Ting et al to the system of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara because the replenishing system ensured sufficient copper ions were present in solution to continue the electroplating process. It would have been obvious to one of ordinary skill in the art to have utilized a single electrolyte storage tank to feed multiple electroplating cells in order to ensure uniformity across the different electroplating cells.

22. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Shinbara (US 6,155,275) as applied above to claims 17-19 and further in view of Uzoh et al (US 6,123,825).

The teachings of Yoshioka et al, Bleck et al and Shinbara are described above. However, none of these references teach that one of the post deposition treatment chambers as a thermal anneal chamber.

Uzoh et al teach (see cols. 7-8) that after formation of an electroplated copper layer on semiconductor wafers, it was customary to perform annealing of the copper layer to ensure small grain size of the copper within the layer.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a conventional post deposition treatment annealing chamber to the system of Yoshioka et al and Bleck et al in order to perform the conventional annealing step to ensure proper grain size of the electroplated copper layer.

Response to Arguments

23. Applicant's arguments filed 17 April 2006 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

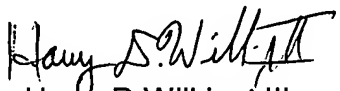
24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry D. Wilkins, III whose telephone number is 571-272-1251. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy V. King can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Harry D Wilkins, III
Primary Examiner
Art Unit 1742

hdw